# EFFICIENT AND FLEXIBLE THYRISTOR CONTROLLED SERIES CAPACITOR SIMULATION IN EMTP – TACS

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**KEY WORDS**

*Flexible AC Transmission Systems (FACTS), Thyristor Controlled Series Capacitor (TCSC), Electromagnetic Transients Program (EMTP), Transient Analysis of Control Systems (TACS)*

## ABSTRACT

*This paper describes an innovative implementation of Thyristor Controlled Series Capacitors (TCSC) models in the EMTP. The TCSC model has been built solely from published information in the technical literature and results have been duplicated. The model can thus be used with confidence as benchmark for validation of less detailed models suitable for planning applications.*

## 1. INTRODUCTION

Fixed series compensation is an established economical technique for increasing the power transfer capability of transmission systems. Series capacitor compensation decreases the effective reactance of the compensated line which means a change in power flow pattern among parallel transmission corridors. Controlled series capacitor (CSC) compensation adds to this possibility the ability to schedule power flows along desired lines and to modulate the effective impedance in response to power system dynamics.

Two forms of CSC have emerged. The thyristor controlled series capacitor (TCSC) [1] [2] has vernier control capability (continuous control) while the thyristor switched series capacitor (TSSC) [3] provides discrete levels of series compensation only. This paper uses TCSC equipment for demonstrating the EMTP modeling approach.

Engineers need analysis tools in order to investigate CSC and evaluate the potential benefits of controlled devices in their power system: transient stability, small signal stability, power flow and short–circuit models for CSC devices are needed. The problem of validating these models is acute. An EMTP model is certainly very useful in coming up with validated simplified model for transient stability programs. An EMTP model is also a requirement for the investigations of subsynchronous resonance problems normally feared when dealing with fixed series compensation.

The paper starts with describing the TCSC equipment and its controls, then model implementation is discussed. Difficulties to model digital controls such as those found in TCSC are presented and it is shown how to reduce the TCSC computation time used by the EMTP –TACS simulation.

## 2. OVERVIEW OF TCSC EQUIPMENT

A TCSC module consists of a series capacitor in parallel with a thyristor switch and reactor. The net series compensation seen by the transmission line is the parallel combination of the thyristor controlled reactor (TCR) and fixed capacitor. A TCSC system can be made up of one or several such modules in series. The TCSC may also be connected to some fixed or conventional series capacitors as part of the overall compensation scheme. Figure 1 shows a general schematic diagram of one TCSC module. Metal oxide varistors (MOV) protect the capacitors.

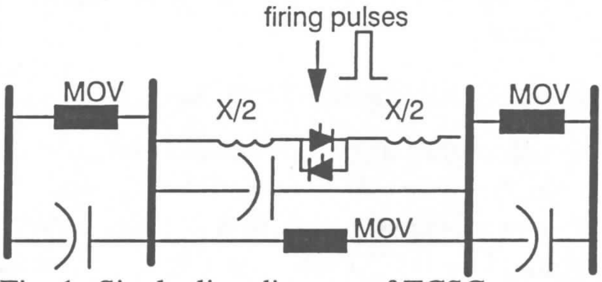



Fig. 1 Single–line diagram of TCSC

Changing the thyristor firing angle (conduction time) changes the fundamental frequency reactance. With the thyristors blocked (zero thyristor conduction time), the TCSC appears as a conventional series capacitor. With the thyristors continuously conducting, the TCSC appears as a small inductance. In principle, the TCSC can operate over a wide range of capacitive and inductive impedances. However the transition from inductive to capacitive is not normally permitted by fast control, due to the L–C oscillations during the transition. Control limits would prevent even temporary operation into the area of resonance.

For a single TCSC module there is a gap in the control range between capacitive and inductive operation, as illustrated in figure 2 [4][5]. In this figure, capacitive and inductive limits are illustrated.

*Overall capacitive reactance limits:* At low line current, the maximum capacitive reactance is limited to a fixed maximum value due to firing angle limitation. At higher line current, the maximum capacitor voltage rating dominates and the maximum reactance limit is inversely proportional to the line current.

*Overall inductive reactance limits:* At low line current, the maximum inductive reactance is restrained to a maximum (fixed) value due to firing angle limitation. At higher line current, the harmonic current heating effect dominates and the maximum reactance limit is inversely proportional to the line current.

With multiple modules it is possible to fill in the gaps in the control range between capacitive and inductive operation. The smoothness of the control range increases with increasing number of modules (combinations of modules of different sizes).

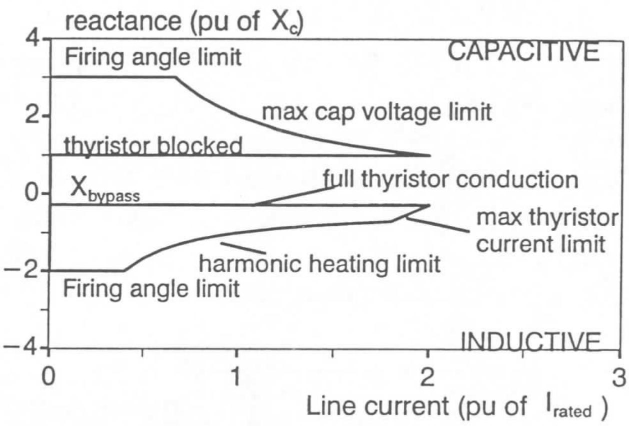



Fig. 2 Typical reactance capability curve of a single TCSC module

## 3. OVERVIEW OF TCSC CONTROL

The TCSC valves conduct on alternate half–cycles of the supply frequency depending on their firing angle $\alpha$ or conduction angle $\sigma$, where $\sigma = 2(\pi - \alpha)$. Then, the control objective is to generate firing pulses controlling $\alpha$, thus the device impedance. A simplified block–diagram of a typical control system is shown in figure 3 [6]. Below is a brief description of the main elements of figure 3.

### Regulator

The regulator module contains basic transfer functions, for example a filter $F_i$ and a PID closed loop regulator.

The control modes include:

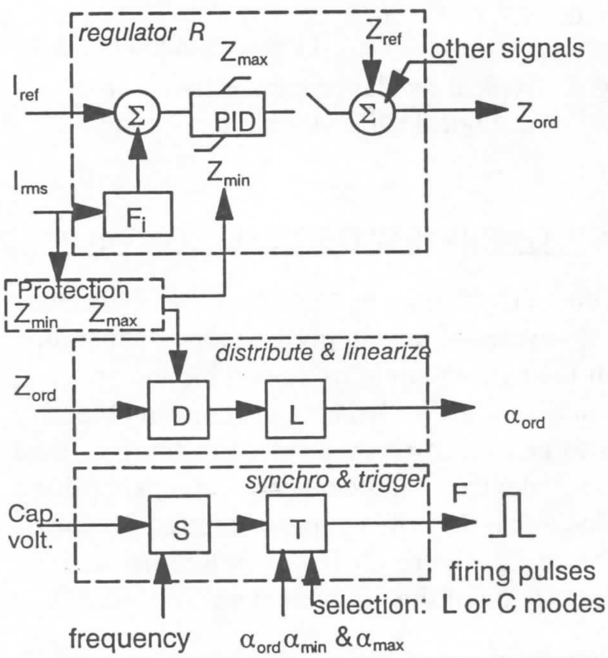
Impedance Control mode (ZC): based upon a reference impedance, the TCSC regulates the angle $\alpha$ through its set value $\alpha_{ord}$, within limits, to maintain a constant impedance. Typically, this is an open loop function.

Current Control mode (CC): based upon a reference current, the TCSC impedance is varied, within limits, to control a constant current on the transmission line. The CC mode is used with regulators feedback, typically PID regulators. Constant power control is also feasible.

Inductive mode (L): full conduction of the thyristors resulting in an inductive impedance of the TCSC.

Capacitive mode (C): blocked thyristors.

The angle $\alpha$ can be controlled to obtain the basic TCSC control modes. Full conduction with $\sigma = 180^o$ is obtained with $\alpha = 90^o$. Partial conduction is achieved with $90^o < \alpha < 180^o$. Firing angles between $0^o$ and $90^o$ are not permitted as they produce asymmetrical currents with dc components.

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|---|---|---|---|
| D | Distribution | R | Regulator |
| F | Firing | S | Synchronization |
| L | Linearization | T | Triggering |

Fig.3: Typical block–diagram of a TCSC current regulator

## Distribution and linearization

The output from the regulator block is a reactance order $Z_{ord}$ which is the input to the distribution unit D. It determines the actual reactance output taking into account the number of modules and different output limits. A linearization function L may be used to supply the firing angle order as a function of the desired reactance. This permits quasi–linear response of a TCSC impedance to control the voltage.

## Synchronizing and triggering

Synchronized trigger signals may be generated independently for each phase, and the synchronization signal may be the capacitor voltage in each phase. Typically, synchronization S uses a phase–locked loop (PLL) oscillator but timing references may use filters to prevent transient and distorted ac system conditions from influencing TCSC operation.

The trigger module T provide pulses for triggering the thyristors in both current directions by comparing the PLL output with $\alpha_{ord}$, constrained between minimum and maximum limits. The firing angle $\alpha$ is the electrical angle between the zero crossing of the synchronizing signal and the instant when the triggering pulse is generated.

## Control limits and protection

*Firing angle limits:* To avoid operating close to resonance, the control system imposes firing angle limits, both in capacitive and inductive operating regions. Hence the full range $90^o < \alpha < 180^o$ is not available. Alternatively, the limitation on the firing angle can be expressed as a reactance limit.

*Capacitive region, Capacitor voltage limits:* The primary protection for the capacitor is the parallel MOV devices. The capacitor voltage is a preferred overload indicator over the TCSC capacitor current because the capacitor current is not sinusoidal and can be larger than the line current depending on the TCR firing angle. There is a time–dependent limit on the maximum operating voltage across the series capacitor. The MOV rating may also impose more severe limitations on capacitor voltages for short duration overvoltages. The maximum voltage limits are translated into maximum reactance limits by dividing the voltage limits with the actual line current. Since the maximum voltage limit is a function of duration and since the line current varies, the calculated reactance limit is dynamic in nature.

*Capacitive region, Capacitor current limits:* At high currents it is necessary to bypass the TCSC to protect the capacitors. The TCSC, once bypassed, has a time delay on reinsertion after the line current falls back below the maximum line current limit.

*Inductive region, Harmonic limits:* The heating effect of TCSC harmonic current flow must be considered. The harmonic content depends on the current flow in the thyristors and the relative sizes of the inductive and the capacitive reactances.

*Inductive region, Thyristor current limits:* When the maximum thyristor current is exceeded, the CSC is bypassed.

## 4. TCSC MODELING IN EMTP–TACS

Modeling of thyristor valves separate from the main EMTP network (representing the ac system in which the TCSC is embedded) has been demonstrated in [7]. This has proven computational time effective in large networks. This paper addresses control system modeling issues, related to both computation time and modeling flexibility.

EMTP simulation of power electronic systems is often characterized by significantly large computation time and the difficulty to model digital control systems, such as those found in TCSC. The reasons are the following.

Typically, control systems such as in figure 3 are modelled in EMTP through TACS. Since TACS is really designed for analog controls, limitations become apparent when modeling digital controls. Fixed–format and free–format TACS pseudo–fortran provide some flexibility towards digital control, but this is limited in terms of functionality. An alternative is MODELS which in some aspects offers more features than TACS. However, both alternatives are modeling languages which translate the control system information into sparse arrays and linked lists to nonlinearity codes, which in the time–step loop are used by the non–iterative solver. There is enough overhead such that large nonlinear control cases are not solved efficiently.

Also, internal delays in the control system solution are the result of the non iterative control system solution. The ordering mechanism is to limit the number of time delays. This is not compatible with digital controls in which the sequence of solution is built in the controls. It will be shown later how ordering mechanism can affect simulation accuracy.

Finally, not all digital controls may be active at each time step. For example, some functions will be enabled when a discrete event occurs. Some functions are solved with small step sizes, while others use a large step size. Furthermore, the solution step size may be different from the integration step size of that used in EMTP.

All these limitations can be alleviated since the TACS user now has the possibility to dynamically link his (her) own executable subroutines in the data file with the EMTP. Each call to a subroutine is interpreted as usage of a device, and this user–defined subroutine is ordered in the solution process. Ordering of the modules can also be by–passed upon request. This remains a flexible way to describe control systems, and it has the advantage of computational efficiency since the overhead is small.

### 4.1 System data

The TCSC implemented in the Kayenta substation, between Navajo and Shiprock, Arizona, has been modelled as shown below. System data and control information have been extracted from [2] and [6]. Figure 4 shows the schematic diagram of Kayenta power substation. The TCSC is located on a 320 kilometer long, 230 kV (60 Hz) transmission line. The ac network itself is small.

Fixed capacitors are divided into sections of 55, and 40 Ohms impedance. The TCSC is 2.6 Ohms inductive and 15 Ohms capacitive. The control system follows the description of figure 3. A step in the TCSC impedance in open loop mode control is the test case in the paper. The final simulation time is 1 sec, and the integration step size is 9,98 μsec.

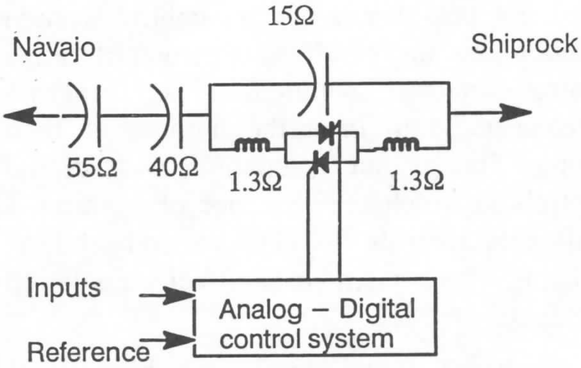


Fig. 4: Schematic diagram of Kayenta sub–station

## 4.2 Plain TACS simulation results

The control system is first modeled with the standard EMTP–TACS instructions, without any enhancements. The representation includes many free–format pseudo–fortran expressions. The TCSC current regulator (regulator block in figure 3 ) is a digital control and it is modelled to mimic this. All the other blocks are analog devices for which TACS is quite flexible.

In this implementation, each function is executed at each time step. The time–loop simulation time obtained on IPC workstation was of 4575.65 sec. Of this total time, the TACS control systems account for 3988 sec, about 87% of the total time.

## 4.3 Dynamically linked control model

To take full advantage of the modeling approach, a complete analog digital control system was developed as a "user–supplied device". TACS elements used are limited to the interface variables and some sources, namely types 11, 90, 91 and some supplemental "88" expression. [9]

In the basic implementation of the user–supplied device, the same EMTP step size is used for all TCSC control elements as we are simply replicating the TACS model. This permits a straight comparison with the plain TACS simulation. The total simulation time (for both the network and the control system) was about 953.28 sec, thus approximately 20% of that for the standard simulation. The control system simulation itself has been speed–up by a factor of about 11. ( 366 sec vs 3988 sec).

The control system simulation time can be reduced even more by taking advantage of the different bandwidths of the control functions. Due to the time constants involved, the regulator function can clearly be solved with a larger step size than that of EMTP. Like in the real system, between solution steps, the output $Z_{ord}$ is held constant. Similarly, not all loops may be activate at each time step.

Another point of interest is that it is not needed to mimic the digital functions. To illustrate this, we consider a stand–alone filter module ($F_i$ module in Fig.3). The module is a group of 4 successive digital filters, the first is an antialiasing one, the second is a band–pass at 60 Hz, the third and fourth are cut–off band–tuned respectively at 120, and 180 Hz. When simulated as per its digital algorithm, the module is executed at a fixed sampling time step which is much larger than the EMTP solution time step (0.521 msec vs 10.42 µsec). With this implementation, not only the accuracy does not suffer, but the simulation is speed–up by a factor of 6 compared to a user–defined model which is merely a plain TACS translation.

## 4.4 Comparison

Figure 5 shows the variation of the thyristor firing angle which was used as disturbance. Figure 6 illustrates the corresponding TCSC capacitor voltage, obtained with the plain TACS – EMTP simulation, while figure 7 represents that obtained with the dynamically linked user–supplied device. The capacitor voltage is where the gap between the results is the largest since it is sensitive to the firing angle. The difference between the results is due to the ordering mechanism in TACS and the time–delays. This has been shown simply by modifying the order in TACS. The user–supplied device uses a more representative ordering when dealing with digital control systems.

Even though there is some sensitivity, the results obtained match published and reliable information. The model can thus be used with confidence as benchmark for validation of less detailed models suitable for planning applications. This can be a complex issue as described in [8] .

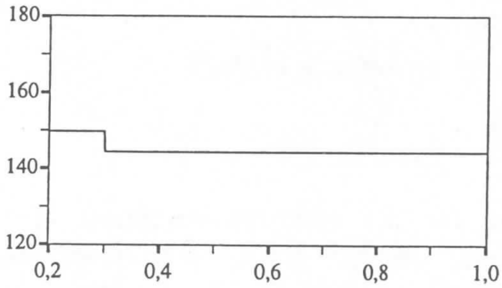


Fig.5: Firing angle ($^0$) vs Time (s)

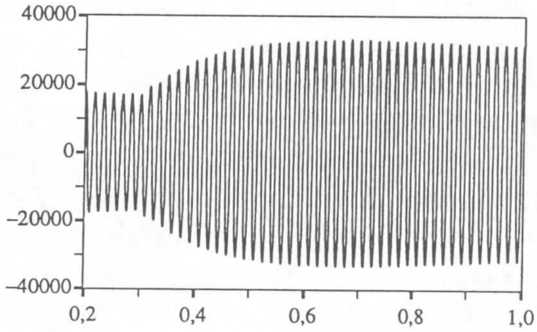


Fig.6: TCSC capacitor voltage (V) vs Time (s); plain TACS simulation

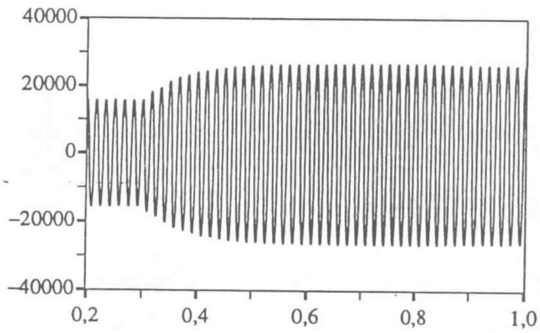


Fig.7: TCSC capacitor voltage (v) vs Time (s); user–supplied model

## 5. CONCLUSION

The paper has shown how significant reduction in EMTP cpu time have been achieved in an EMTP investigation of Thyristor Controlled Series Capacitors, without impacting modeling flexibility. The changes are associated with algorithmic and modeling issues. The TCSC model has been built solely from published information in the technical literature and results have been duplicated.

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