On Control and Balancing of Rigid Bipolar MMC-HVdc Links Enabling Subsystem-Independent Power Transfer

C. Hirsching, M. Goertz, M. Suriyah, T. Leibfried
Institute of Electric Energy Systems and High-Voltage Technology (IEH)
Karlsruhe Insitute of Technology (KIT)
Karlsruhe, Germany
carolin.hirsching@kit.edu

S. Wenig, S. Beckler
TransnetBW GmbH
Stuttgart, Germany
s.wenig@transnetbw.de

***Abstract*—High voltage direct current transmission schemes equipped with modular multilevel converter technology are considered in several realized and planned bulk power transmission projects. Especially in the case of dc cable links with high system lengths, the rigid bipolar configuration presents a suitable compromise between power rating, cost-efficiency and converter redundancy. Caused by the absence of a metallic return path, system degrees of freedom are reduced in contrast to the bipolar configuration with dedicated metallic return. Therefore, the dc currents in positive and negative bipolar subsystem are not independent. This leads to new challenges and motivates the development of advanced control and balancing concepts for rigid bipolar schemes. This paper focuses on balanced and unbalanced ac grid operating conditions with subsystem-independent active power set points in an ac split-busbar scenario, which has not yet been covered in literature. In order to validate the presented methodology, case studies are performed in electromagnetic transient software.**

***Index Terms*—converter control design, EMT, MMC-HVdc, rigid bipolar configuration.**

I. Introduction

In recent years, high voltage direct current transmission links equipped with state-of-the-art modular multilevel converter (MMC-HVdc) technology became an important technical resource in order to cover bulk power transmission requirements [1], [2]. HVdc projects realized and planned with cable transmission increased in the last years [3] and are recently also taken into consideration for onshore interconnectors due to a higher social acceptance in contrast to overhead-line realizations.

Regarding HVdc cable systems with high system lengths, a bipolar configuration without dedicated metallic return (DMR) cable, also known as rigid bipolar configuration, combines economic advantages, high transmission capacity as well as converter redundancy in terms of reconfiguration capability to an asymmetric monopole during converter maintenance or converter-internal faults. A bipolar configuration with earth return as well saves additional cable costs, but is not taken into account in most parts of the world due to ecological reasons.

The rigid bipolar configuration is depicted in Fig. 1. In contrast to the bipolar configuration with DMR only one dc side current loop instead of two exists in rigid bipolar configuration during normal operation. Therefore, the amount of dc side degrees of freedom is reduced, which causes challenges in control design. Currently, some interconnector projects are in construction and planning stage [4]-[6] and are designed to operate with balanced voltage levels in both bipolar subsystems [4]. Control and balancing aspects for this operation mode have been provided in previous research [7]. Regarding the ac grid connection of an HVdc link in rigid bipolar configuration it could be of operational interest that ac busbars of positive and negative converter are connected to different points of common coupling (PCC). Within this context the transmission of different active power levels in each bipolar subsystem, as depicted in Fig. 1, reveals a new operation mode in rigid bipolar schemes. This contribution discloses the challenges of rigid bipolar HVdc systems operating with different active power set points in each bipolar subsystem and provides a control and balancing scheme to realize operation in this mode.

The remainder of this paper is organized as follows. Section II introduces MMC control basics as well as an improved power and energy balancing concept to guarantee stable operation in an ac split-busbar scenario with different active power levels. Moreover, the applicability of the introduced operation mode for utilization of different submodule types, namely half-

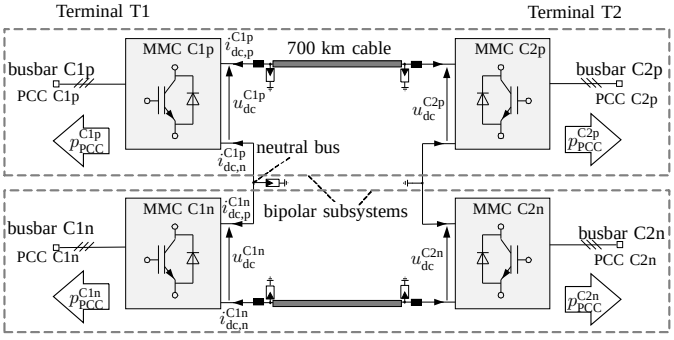

Fig. 1. Rigid bipolar HVdc transmission scheme

bridge and full-bridge-type submodules, is elaborated and an adaptive dc voltage control scheme to guarantee requested power set points is provided. In section III the introduced methodology is validated for a balanced case study as well as an ac contingency in electromagnetic transients (EMT) software, whereas section IV concludes the paper.

II. Rigid bipolar HVDC scheme

In Fig. 2, a MMC terminal in rigid bipolar configuration is depicted. Each terminal Tx, $x\epsilon\{1,2\}$ consists of a positive and a negative converter Cxs, $s\epsilon\{\text{p,n}\}$. The busbar between both converters is defined as the neutral bus, where several dc grounding conditions appear feasible (depicted as box G in Fig. 2) [8]. Within this contribution, a single-point grounded rigid bipolar transmission scheme is investigated (see Fig. 1). The grounding resistance at the dc voltage-controlled terminal T2 is considered as 1 Ω, whereas the neutral bus of the dc current-controlled terminal T1 is connected to a neutral bus surge arrester. MMCs are modelled utilizing type-4 detailed equivalent models according to the classification in [9]. Submodules are primarily considered as full-bridge-type to enable flexible adaption of the converter dc voltage [2]. As explained later, this is a key element for subsystem-independent active power transmission.

A. MMC control basics

By means of mesh analysis similar to [1], [7], [10] and [11], the following equations are derived from Fig. 2 for each phase $y\epsilon\{1,2,3\}$ at the positive converter Cxp.

$$u_{\text{conv},y}^{\text{C}x\text{p}} + L_{\text{arm}} \cdot \frac{\text{d}}{\text{d}t} i_{\text{p},y}^{\text{C}x\text{p}} + u_{\text{p},y}^{\text{C}x\text{p}} - u_{\text{dc}}^{\text{C}x\text{p}} - u_{\text{m},0}^{\text{T}x} = 0 \quad (1)$$

$$u_{\text{conv},y}^{\text{C}x\text{p}} - L_{\text{arm}} \cdot \frac{\text{d}}{\text{d}t} i_{\text{n},y}^{\text{C}x\text{p}} - u_{\text{n},y}^{\text{C}x\text{p}} - u_{\text{m},0}^{\text{T}x} = 0 \quad (2)$$

The phase module current $i_{\text{phm},y}$ is introduced in (3) for each phase.

$$i_{\text{phm},y}^{\text{C}x\text{p}} = \frac{i_{\text{p},y}^{\text{C}x\text{p}} + i_{\text{n},y}^{\text{C}x\text{p}}}{2} \quad (3)$$

Now, calculating [(2)+(1)]/2 and [(2)-(1)]/2 results in system equations (4) and (5), respectively. Here, arm delta voltage $u_{\Delta,y}$ and arm sum voltage $u_{\Sigma,y}$ are defined. Superscript Cxp is neglected in the following as system equations are valid for all four MMCs within the rigid bipolar transmission scheme.

$$u_{\Delta,y} = \frac{u_{\text{n},y} - u_{\text{p},y}}{2} = \frac{L_{\text{arm}}}{2} \frac{\text{d}}{\text{d}t} i_{\text{conv},y} + u_{\text{conv},y} + u_{\text{offset}} \quad (4)$$

$$u_{\Sigma,y} = \frac{u_{\text{p},y} + u_{\text{n},y}}{2} = -L_{\text{arm}} \frac{\text{d}}{\text{d}t} i_{\text{phm},y} + \frac{u_{\text{dc}}}{2} \quad (5)$$

Whereas (4) represents the ac side system dynamics of an MMC, (5) reflects internal and dc side dynamics. Decomposition of each converter into its decoupled ac and dc side quantities allows for independent control design of ac and dc side. The offset u_{offset} in (4) includes $u_{\text{dc}}/2$ as well as neutral bus voltage $u_{\text{m},0}^{\text{T}x}$. Regarding more detailed ac side control design the reader is further referred to [10]. Now, focusing on dc side control design, transformation of (5) into stationary reference frame reveals the zero component system dynamics in (6) for each of the four converters Cxs within the rigid bipolar transmission scheme:

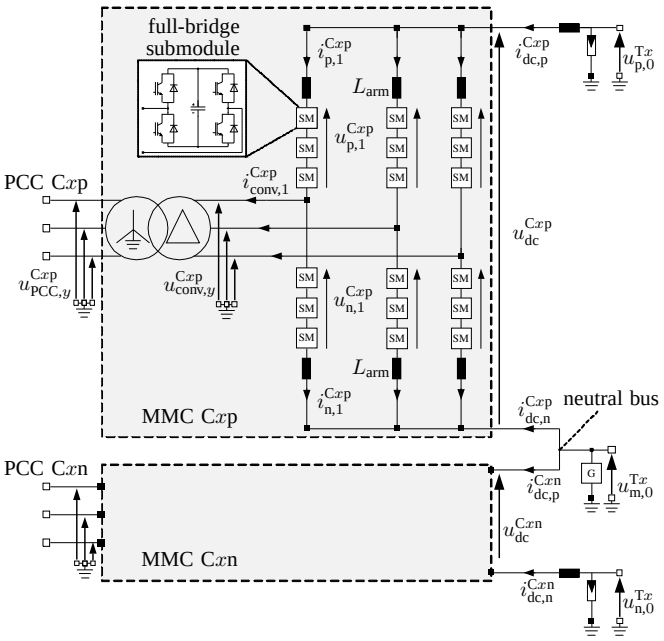

Fig. 2. Three phase equivalent circuit of a single MMC terminal in rigid bipolar configuration

$$u_{\Sigma,0}^{\text{C}xs} = -L_{\text{arm}} \cdot \frac{\text{d}}{\text{d}t} i_{\text{phm},0}^{\text{C}xs} + \frac{u_{\text{dc}}^{\text{C}xs}}{2}. \quad (6)$$

It should be noticed that the converters dc current corresponds to $i_{\text{dc,p}}^{\text{C}xs} \propto 3 \cdot i_{\text{phm},0}^{\text{C}xs}$ in steady-state. Generally, dc side quantities are adjusted by $u_{\Sigma,0}^{\text{C}xs}$. Therefore, (6) obviously highlights one dc side degree of freedom per converter in bipolar configuration with DMR or rather four dc side degrees of freedom per dc link. The main difference between rigid bipolar configuration and bipolar configuration with DMR is the absence of the metallic return path. The dc voltages in each of two bipolar subsystems may differ in both types of bipolar configuration. However, in rigid bipolar configuration the relations $i_{\text{dc,p}}^{\text{C}x\text{p}} = i_{\text{dc,p}}^{\text{C}x\text{n}}$ as well as $i_{\text{phm},0}^{\text{C}x\text{p}} = i_{\text{phm},0}^{\text{C}x\text{n}}$ exist as long as the neutral bus arrester is in non-conducting state. Summarizing two controllable dc voltage levels, but only one controllable dc current in contrast to the bipolar configuration with DMR, highlights that dc side degrees of freedom are reduced from four to three in rigid bipolar configuration. These are adjustable by the four control values $u_{\Sigma,0}^{\text{C}xs,*}$. It becomes apparent that dc side quantities in positive and negative bipolar subsystem can not be controlled independently within rigid bipolar configuration. In [7], an averaged control approach was chosen for terminal-wide dc current and dc voltage control. The third dc side degree of freedom was disregarded in control design to avoid communication requirements between both terminals.

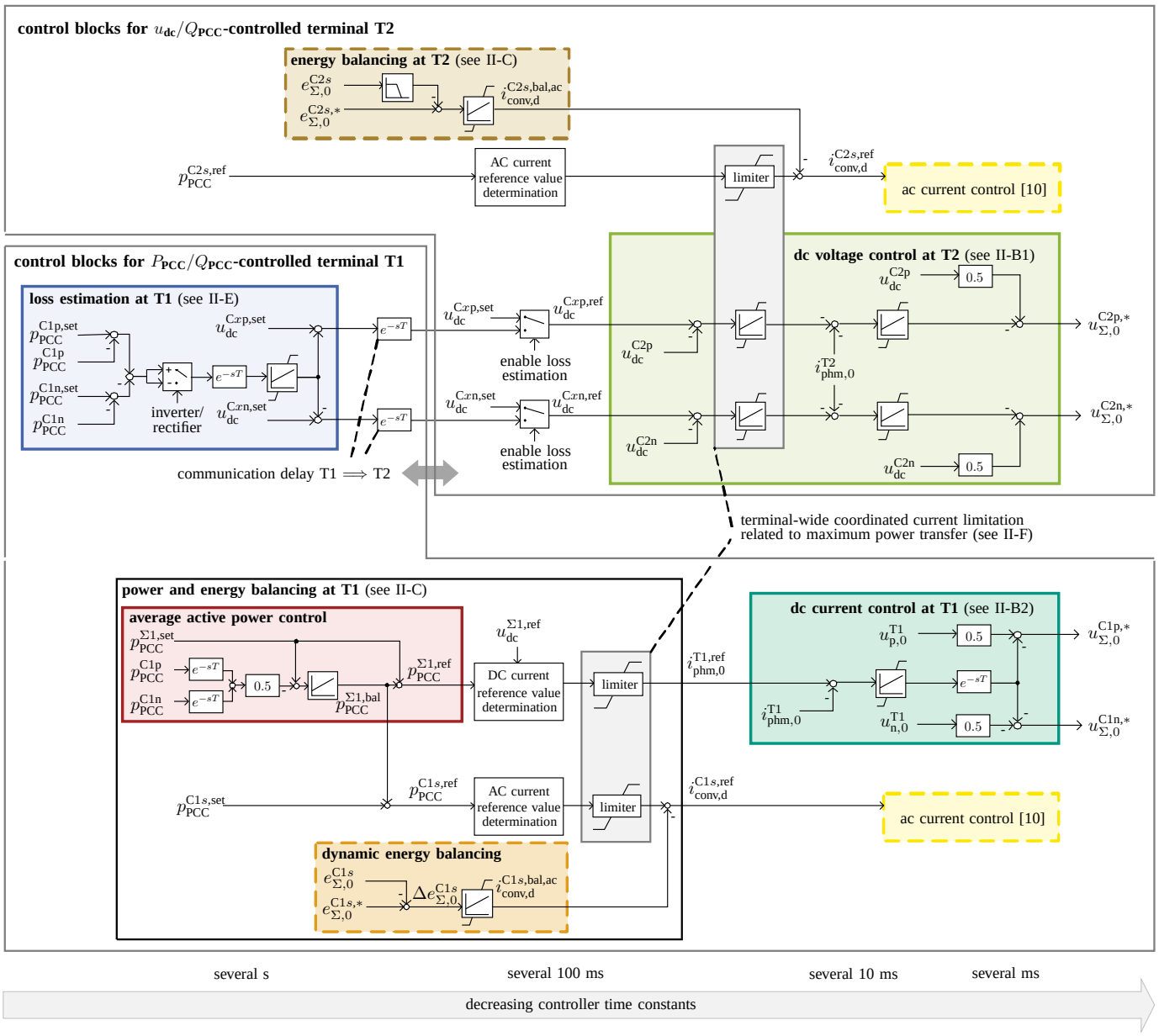

Fig. 3. Control and balancing scheme for transmission of different active power levels in each bipolar subsystem in rigid bipolar configuration. Main control blocks are shown for P_{PCC}/Q_{PCC}-controlled terminal T1 as well as u_{dc}/Q_{PCC}-controlled terminal T2. Solid boxes represent terminal-wide realized controls and dashed boxes show MMC-internal control blocks.

As ac side controls are decoupled from dc side controls, converters in the positive and negative subsystem could be connected to different PCCs, due to spatial restrictions or systemic requirements. This is defined as an ac split-busbar scenario. Within this scenario, as depicted in Fig. 1, the transmission of different active power levels $p_{PCC}^{Cxp} \neq p_{PCC}^{Cxn}$ in each bipolar subsystem might be of operational interest. This operating case requires the development of an advanced control and balancing scheme, which is introduced in this contribution. The main control blocks in order to determine the four dc side control values $u_{\Sigma,0}^{Cxs,*}$ at terminals T1 and T2 are depicted in Fig. 3. The control blocks are arranged from left to right starting from highest to lowest time constant as indicated at the bottom. All control blocks are explained in detail within the following sections.

B. Dc side controls for subsystem-independent power transfer

In an ac split-busbar scenario with different active power levels in each bipolar subsystem, the averaged dc side control approach introduced in [7] is not applicable. Therefore, an adapted dc side control structure is introduced for this operation mode. Reminiscing the fact that positive and negative bipolar subsystem represent one dc current circuit, one of the three dc side degrees of freedom is related to the dc current control loop. The remaining two degrees of freedom

are utilized to set different dc pole-to-ground voltage levels related to the requested active power level in each bipolar subsystem. Therefore, communication between both terminals is required.

1) Dc voltage control: Within this contribution, terminal T2 is dc voltage-controlled. The light green colored box in Fig. 3 presents a cascaded control structure for dc voltage control. In this section, converters in positive and negative subsystem receive independent dc voltage set points $u_{\mathrm{dc}}^{\mathrm{C}xs,\mathrm{set}}$ as reference values $u_{\mathrm{dc}}^{\mathrm{C}xs,\mathrm{ref}}$. These are proportional to the active power level requested for the respective bipolar subsystem at terminal T1 and demand for communication between both terminals, even though loss estimation block / blue colored box in Fig. 3 is deactivated. Within the inner control loop, different voltage levels in each bipolar subsystem are then realized by feeding forward of the respective dc voltage $u_{\mathrm{dc}}^{\mathrm{C}xs}$. Here, the terminal phase module current zero component $i_{\mathrm{phm},0}^{\mathrm{T}x}$ is introduced, which corresponds to the phase module current component flowing through positive and negative converter. In general, terminal-wide defined variables (superscript T) are obtained by averaging the signals of positive and negative converter under consideration of a communication dead time of 40 μs.

2) Dc current control: In [7], an averaging control approach was introduced at the dc current-controlled terminal T1. When considering different active power levels, different dc pole-to-ground voltages are set by terminal T2 in each bipolar subsystem. Application of the averaged control approach, which includes feeding forward of the average dc voltage, would lead to a voltage shift $|u_{\mathrm{m},0}^{\mathrm{T1}}| > 0$ kV of the floating neutral bus at terminal T1. Therefore, the averaging control approach is adapted as depicted in Fig. 3 (dark green colored box). The dc current $i_{\mathrm{phm},0}^{\mathrm{T1}}$ is controlled terminal-wide depending on the average subsystem power demand, which is determined within the outer control loops (red colored control block in Fig. 3). But, control values $u_{\Sigma,0}^{\mathrm{C1}s,*}$ are then obtained independently by feeding forward of the respective dc pole-to-ground-voltage $u_{s,0}^{\mathrm{C1}s}$ for positive and negative converter. Thus, potential $u_{\mathrm{m},0}^{\mathrm{T1}}$ of the floating neutral bus at terminal T1 remains approximately at 0 kV.

C. Power and energy balancing scheme for subsystem-independent active power transfer

As described by (7), the average arm energy change $\dot{e}_{\Sigma,0}$ is decomposable into components transferred from the dc side (p_{dc}) to the ac side (p_{ac}) under consideration of internal losses (p_{loss}) [11]. Moreover, the average arm energy change is characterized by a steady-state component $\bar{\dot{e}}_{\Sigma,0}$ as well as a dynamic energy component $\tilde{\dot{e}}_{\Sigma,0}$.

$$\dot{e}_{\Sigma,0} = \frac{1}{6}\left(p_{\mathrm{dc}} + p_{\mathrm{loss}} - p_{\mathrm{ac}}\right) \approx \underbrace{\bar{\dot{e}}_{\Sigma,0}}_{\bar{p}_{\Sigma,0}} + \tilde{\dot{e}}_{\Sigma,0} \tag{7}$$

Within a bipolar HVdc scheme with DMR, balancing of total energy requirements within the MMCs is realized in two ways according to [10] assuming $\bar{\dot{e}}_{\Sigma,0} \gg \tilde{\dot{e}}_{\Sigma,0}$:

- balancing via the dc side (p_{dc}) by adaption of the dc current reference value by a balancing component $i_{\mathrm{phm},0}^{\mathrm{bal,dc}}$ depending on the MMCs total energy requirements. In order to guarantee the requested power at the PCC, this option was chosen for the dc current-controlled terminal.
- balancing via the ac side (p_{ac}) by adaption of the ac current direct component by a balancing component $i_{\mathrm{conv,d}}^{\mathrm{bal,ac}}$ at the dc voltage-controlled terminal.

In a rigid bipolar terminal, ac side dynamics of both converters operate independently. Therefore, balancing of energy requirements towards the ac side as described is still applicable for the dc voltage-controlled terminal T2 (see brown colored box in Fig. 3).

Now, focusing on the dc current-controlled terminal, the following considerations have to be taken into account: modulation methods and switching operations of power electronic devices are performed individually in both converters. Consequently, the instantaneous value of the energy requirements at positive and negative converter may differ. Since both converters are series-connected to one dc current circuit, balancing of the respective energy demand via a subsystem-independent dc current balancing component is not feasible. On the other hand, balancing of the total energy demand per converter via the ac side would lead to a stationary deviation between the transferred power $p_{\mathrm{PCC}}^{\mathrm{C1}s}$ and the requested power $p_{\mathrm{PCC}}^{\mathrm{C1}s,\mathrm{set}}$ at the PCC. In [7], total energy balancing was therefore proposed to be realized at two different time scales: $i)$ slow timescale: compensation of the average steady-state losses $\bar{p}_{\Sigma,0}$ via the dc side by adaption of the terminal phase module current $i_{\mathrm{phm},0}^{\mathrm{T1}}$, $ii)$ fast timescale: compensation of instantaneous converter-internal energy differences $\Delta e_{\Sigma,0}^{\mathrm{C}xs} \approx \tilde{e}_{\Sigma,0}$ via the ac side independently for each converter by adaption of the active ac current $i_{\mathrm{conv,d}}^{\mathrm{C1}s}$.

Here, the power and energy balancing concept introduced in [7] is adapted for subsystem-independent power transfer as depicted in Fig. 3 (see black-edged box with red and orange colored control blocks). Signals denoted with superscript Σ are obtained by averaging the respective signal of positive and negative converter under consideration of a signal delay of 40 μs. In contrast to signals with denotation T, these signals are artificial and without any physical meaning in a scenario with subsystem-independent active power transfer. By means of the averaged subsystem losses, a power balancing component $p_{\mathrm{PCC}}^{\Sigma 1,\mathrm{bal}}$ is determined to obtain the averaged power reference of the terminal $p_{\mathrm{PCC}}^{\Sigma 1,\mathrm{ref}}$. This results in an adaption of the dc current to compensate the steady-state terminal losses via the dc side (see Fig. 3, red colored box). The amount of power to compensate steady-state terminal losses is distributed to positive and negative converter depending on the respective converter dc voltage $u_{\mathrm{dc}}^{\mathrm{C1}s}$. However, dc voltage levels $u_{\mathrm{dc}}^{\mathrm{C1}s}$ at terminal T1 are not proportional to the active power level within the respective bipolar subsystem when transmission losses are disregarded. Therefore, the steady-state losses of the converter with reduced active power level are under-compensated while losses of the other converter are over-compensated. However, deviation of transmitted and requested

power at the PCC is lower than in case of total energy balancing via the ac side. Remedy may serve an adaptive dc voltage control as proposed in section II-E.

Since the ac side outer control loops depend on the power reference value of the particular converter $p_{\mathrm{PCC}}^{\mathrm{C}xs,\mathrm{ref}}$, this is determined individually for each converter during operation with subsystem-independent active power transmission. In order to obtain $p_{\mathrm{PCC}}^{\mathrm{C1}s,\mathrm{ref}}$ at converter C1s, the requested active power set point $p_{\mathrm{PCC}}^{\mathrm{C1}s,\mathrm{set}}$ is feed-forwarded to the terminal-wide determined balancing component $p_{\mathrm{PCC}}^{\Sigma 1,\mathrm{bal}}$. Compensation of volatile energy deficits as well as remaining stationary losses is realized individually for both converters via the ac side (see Fig. 3, orange box).

D. Limitation of subsystem-independent active power transfer for utilization of half-bridge submodules

Within this section, applicability of the introduced methodology to transfer different active power levels in each bipolar subsystem is elaborated for the utilization of full-bridge-type as well as half-bridge submodules.

The characteristic of a full-bridge-type submodule to provide negative submodule voltages enables the implementation of dc fault ride through (FRT) sequences and establishes its fault current interruption capability. Another advantage of this characteristic is that a decrease of the valve-side ac voltage is not required when reducing the dc voltage level for lower power transmission. Therefore, submodule current limits are not attained at typical system design and transferred power per subsystem is theoretically adjustable in a flexible manner. However, protection criteria e.g. for over-voltage or under-voltage detection have to be adapted for this operation mode.

In MMCs equipped with half-bridge (HB) submodules (HB-MMC), reduction of transferred power from nominal power is limited by the fact that HB submodules are not able to provide negative output voltages. The valve-side ac voltage $u_{\mathrm{conv},y}$ is decomposable into an oscillating part with a peak voltage $\hat{U}_{\mathrm{conv}}$ as well as a dc offset with an absolute value of approximately $u_{\mathrm{dc}}/2$. Within a HB-MMC the dc voltage u_{dc} has to be rated higher than the maximum absolute value of the valve-side ac voltage $\hat{U}_{\mathrm{conv}} + u_{\mathrm{dc}}/2$. This corresponds to the relation $2\hat{U}_{\mathrm{conv}} < u_{\mathrm{dc}}$, therefore, the minimum dc voltage equals $2\hat{U}_{\mathrm{conv}}$ in a bipolar HVdc system with HB-MMCs. Moreover, the current stress within the submodules increases with reduced valve-side rated ac voltage $u_{\mathrm{r,conv}}$ when transmitting nominal power. The arm current $i_{s,y}$ is decomposable into a dc component of approximately $i_{\mathrm{phm},0}$ and an oscillating part with peak current $\hat{I}_{\mathrm{conv}}/2$. The dc component is approximated by the active power level P_{conv} and corresponding dc voltage level of the MMC. The oscillating part depends on apparent power S_{conv} of the MMC and the valve-side rated ac voltage. When disregarding internal current loops, the maximum arm current $|i_{s,y,\mathrm{max}}|$ is approximated by (8). For more detailed design aspects the reader is further referred to [1] and [12].

$$|i_{s,y,\mathrm{max}}| \approx i_{\mathrm{phm},0} + \frac{\hat{I}_{\mathrm{conv}}}{2} = \frac{P_{\mathrm{conv}}}{3u_{\mathrm{dc}}} + \frac{\sqrt{2}S_{\mathrm{conv}}}{2\sqrt{3}u_{\mathrm{r,conv}}} \qquad (8)$$

TABLE I
ESTIMATION OF MINIMUM DC VOLTAGE, MAXIMUM ARM CURRENT AND CORRESPONDING ACTIVE POWER DIFFERENCE BETWEEN SUBSYSTEMS IN A 525 KV RIGID BIPOLAR HB-MMC HVDC SCHEME.

$u_{\mathrm{r,conv}}$	$u_{\mathrm{dc,min}}$	$p_{\mathrm{diff,max}}$	$\lvert i_{s,y,\mathrm{max}}^{p\downarrow}\rvert$	$\lvert i_{s,y,\mathrm{max}}^{p\uparrow}\rvert$
160 kV	261 kV	≈ 50 %	2.4 kA	**3.5 kA**
220 kV	359 kV	≈ 30 %	2.2 kA	**2.8 kA**
320 kV	523 kV	≈ 0 %	2.1 kA	

Now, the consideration of operational safety margins reveals that reduction of active power transmission within one bipolar subsystem is feasible to a limited extent with HB-MMCs. Table I provides an estimation of the minimum feasible dc voltage $u_{\mathrm{dc,min}}$ depending on the valve-side rated ac voltage. In addition, the maximum possible power difference $p_{\mathrm{diff,max}}$ between positive and negative bipolar subsystem is estimated for a 525 kV HVdc system. Moreover, the arm current stresses $|i_{s,y,\mathrm{max}}^{p\downarrow}|$ and $|i_{s,y,\mathrm{max}}^{p\uparrow}|$ are estimated for corresponding reduced active power transmission ($p\downarrow$) and nominal power transmission ($p\uparrow$), respectively (rated active and reactive power per MMC: $P_{\mathrm{r}} = 1050$ MW, Q_{r} = +400 MVAr). It should be noted that these exemplary calculations do not consider any safety margins nor third harmonic voltage injection.

In summary, the extent of $p_{\mathrm{diff,max}}$ within a HB-MMC is mainly a design aspect of converter ac voltage and ampacity of power electronic devices (red marked current ratings in Table I are not covered by state-of-the-art MMC submodules). Application of tap changers at the converter transformers could increase the usable ac voltage band and consequently the utilisation factor of HB-MMC topologies. Moreover, hybrid MMCs equipped with half-bridge as well as full-bridge-type submodules may present a feasible compromise to combine greater active power transmission flexibility, dc fault current interruption as well as dc fault-ride through capability, reasonable power electronic losses and overall cost-effectiveness.

E. Adaptive dc voltage control for subsystem-independent active power transfer

As elaborated in section II-C, a stationary deviation $\Delta p_{\mathrm{PCC}}^{\mathrm{C1}s}$ between requested and delivered power arises at the PCCs of the $P_{\mathrm{PCC}}/Q_{\mathrm{PCC}}$-controlled terminal when realizing different active power levels in each bipolar subsystem. Compensation of terminal losses at fixed dc voltage levels leads to a positive deviation $+\Delta p_{\mathrm{PCC}}^{\mathrm{C1}s}$ at the PCC of greater active power transfer and a negative deviation $-\Delta p_{\mathrm{PCC}}^{\mathrm{C1}s}$ at the other one. This behavior is traced back to transmission losses, which present a significant proportion of subsystem losses in HVdc links with high system lengths [13]. Earlier, this kind of losses were not regarded when setting the dc voltage levels per subsystem. Here, a methodology is developed to estimate the transmission losses and compensate the respective power deviation $\Delta p_{\mathrm{PCC}}^{\mathrm{C1}s}$ by an appropriate adaption of the reference dc voltage per subsystem.

The proposed transmission loss estimation scheme is depicted in Fig. 3 (see blue colored box). Here, $u_{\mathrm{dc}}^{\mathrm{C}xs,\mathrm{set}}$ is

defined as the dc voltage operating point, which is determined proportional to the active power level in the respective bipolar subsystem. In section II-C this signal was set equal to the respective reference dc voltage $u_{\mathrm{dc}}^{\mathrm{C}xs,\mathrm{ref}}$. Now, transmission losses as well as the respective active power level are considered in order to determine adequate dc voltage levels. By means of an overlaid control scheme with a sufficiently high time constant compared to averaged active power control, a voltage component is determined to adapt the reference dc voltage within each bipolar subsystem (a communication delay of 3.5 ms between both terminals is taken into account). This results in a slightly reduced dc voltage level $u_{\mathrm{dc}}^{\mathrm{C}xs,\mathrm{ref}}$ within the subsystem of higher active power transfer and a corresponding increased dc voltage level within the other subsystem. The extent of voltage adaption should be tightly limited.

Due to the adaption of dc voltage levels, the power and energy balancing methodology proposed earlier operates in the desired manner. Steady-state terminal losses are compensated completely via the dc side and the amount of terminal balancing power $p_{\mathrm{PCC}}^{\Sigma 1,\mathrm{bal}}$ is distributed appropriately to positive and negative converter according to their adapted dc voltage levels. Therefore, the power deviation $\Delta p_{\mathrm{PCC}}^{\mathrm{C}1s}$ vanishes at both PCCs. Instantaneous energy differences, which are caused by differing energy requirements in both converters, are balanced via the ac side, but are orders of magnitudes smaller than in the case without line loss estimation.

F. Control design and limiter coordination

It is indicated in Fig. 3 that control blocks are arranged with decreasing time constants from left to right. The inner ac current controller (see Fig. 3, yellow boxes) is designed by modulus optimum method. Controller plant characteristics are derivable from Table II.

The inner dc current controllers (see Fig. 3, inner controller of light green box as well as dark green box) are designed by utilization of structured feedback gains. Regarding more detailed dc side control design the reader is further referred to [11]. Resulting controller outputs of dc current controllers are the control values $u_{\Sigma,0}^{\mathrm{C}xs,*}$. Limitation of inner dc current controllers is set to $\pm\frac{u_{\mathrm{dc,r}}}{2}\cdot\kappa_1$, whereas κ_1 is set to 1.1.

It is important to ensure that cascaded controllers are designed to operate decoupled from each other. Therefore, the outer controllers are designed by application of the symmetrical optimum method. In order to minimize overall system losses, the line loss estimation block (see blue colored box in Fig. 3) should be tightly limited. Here, controller limits are implemented by $\pm u_{\mathrm{dc,r}}\cdot\kappa_2$, whereas κ_2 is set to 0.025. The output of the power controller is not limited (see red colored boxes in Fig. 3), but reference values for the inner controllers are limited by a terminal-wide coordination scheme (see grey boxes in Fig. 3).

Current limits have to be coordinated based on the ampacity of power electronic devices taking into account all decoupled current components. Regarding state-of-the-art submodules an arm current peak value limit of 2.5 kA is chosen. As elaborated in section II-D, the arm current is decomposable into an ac component of approximately $\frac{i_{\mathrm{conv}}}{2}$ as well as a dc component $i_{\mathrm{phm,0}}=\frac{i_{\mathrm{dc}}}{3}$. Related to the converter specification stated in Table II the limit of the valve side ac current peak value is set to ± 3 kA, taking into account an existing balancing component margin required during steady-state operation. In order to rely on the previously defined current limits of the submodules, limitation of $i_{\mathrm{phm,0}}^{\mathrm{T}x,\mathrm{ref}}$ is set to ± 1 kA. Energy balancing current components are limited independently from power flow related ones (see orange and brown boxes in Fig. 3). During FRT sequences fulfillment of energy balancing requirements represent a major challenge due to severe operation point changes. For such an event, zero remaining active power transmission ($i_{\mathrm{phm,0}}\approx 0$) and simultaneous reactive current injection with respect to chosen limits is regarded. Therefore, the limitation of $i_{\mathrm{conv,d}}^{\mathrm{C}1s,\mathrm{bal,ac}}$ should be in the range of ± 1.8 kA to remain within the earlier mentioned system boundaries under consideration of a small margin.

TABLE II
DESIGN PARAMETER SET FOR A 525 KV HVDC LINK IN RIGID BIPOLAR CONFIGURATION

Parameters	**Value**
rated dc voltage (pole to ground) $u_{\mathrm{dc,r}}$	$\pm$ 525 kV
rated ac voltage (valve- / grid-side)	320 kV / 400 kV
rated MMC apparent power $S_{\mathrm{conv,r}}^{\mathrm{C}xs}$	1300 MVA
rated power dc link	2.1 GW
nominal dc current $i_{\mathrm{dc,nom}}$	2.1 kA
nominal ac current $i_{\mathrm{conv,nom}}^{\mathrm{C}xs}$	2.1 kA
arm / transformer short circuit inductor	50 mH / 80 mH
average submodule stack voltage	675 kV (270 · 2.5 kV)
submodule capacitor	8.5 mF

TABLE III
PARAMETER SET FOR A 525 KV HVDC LINK IN RIGID BIPOLAR CONFIGURATION IN AN AC SPLIT-BUSBAR SCENARIO WITH SUBSYSTEM-INDEPENDENT POWER TRANSFER

Parameters	**Value**
power operating points (C1p / C1n)	1050 MW / 350 MW
dc voltage set points (Cxp / Cxn)	525 kV / 175 kV
reactive power levels (Cxs)	+400 MVAr
SCL / SCR / frequency ac grid	45 GVA / 10 / 50 Hz
neutral bus arrester protective level	150 kV

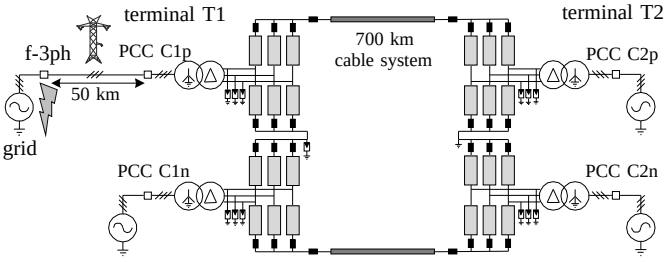

Fig. 4. Rigid bipolar HVdc link in an ac split-busbar scenario with fault location f-3ph in the vicinity of PCC C1p

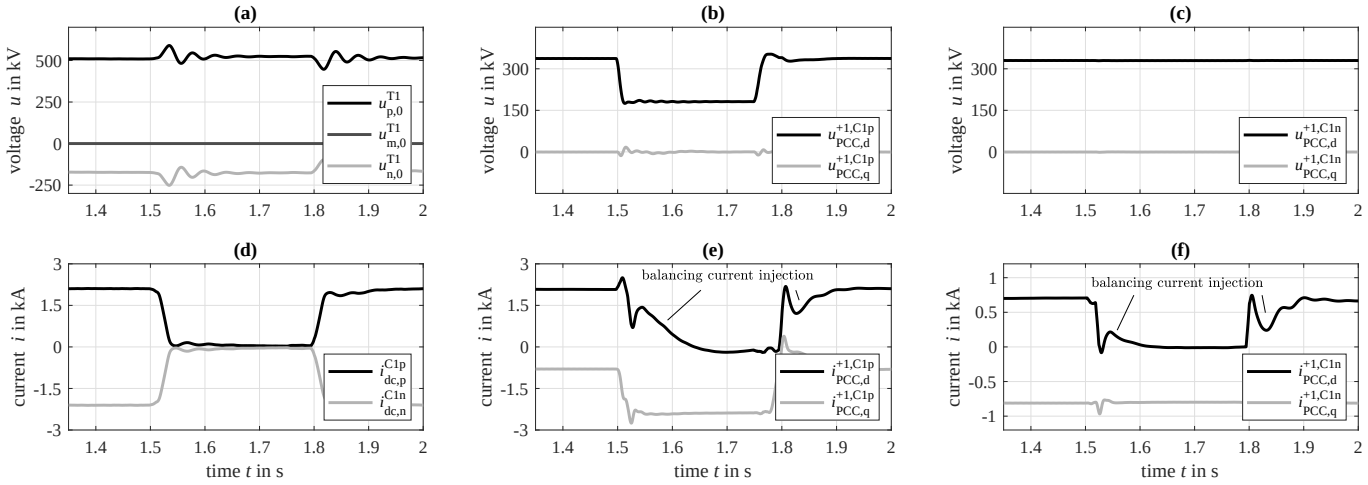

Fig. 5. Response of a rigid bipolar link with subsystem-independent power transfer to an AC three-phase-to-ground fault in the vicinity of PCC C1p: (a) dc voltages at T1, (b) dq-voltages at PCC C1p, (c) dq-voltages at PCC C1n, (d) dc currents at T1, (e) dq-currents at PCC C1p, (f) dq-currents at PCC C1n.

III. Case Study

The introduced methodology to transfer different active power levels in each bipolar subsystem is now validated within an EMT simulation environment according to the scenario depicted in Fig. 4. Tables II and III list the HVdc link design parameters. Here, MMCs are equipped with full-bridge-type submodules and an active power level of $p_{\mathrm{PCC}}^{\mathrm{C1n,set}} = 350$ MW is set as operation point of the negative converter at T1. The active power level of the positive converter is set to nominal power $p_{\mathrm{PCC}}^{\mathrm{C1p,set}} = 1050$ MW. The corresponding dc voltage set points are $u_{\mathrm{dc}}^{\mathrm{C1p,set}} = 525$ kV and $u_{\mathrm{dc}}^{\mathrm{C1n,set}} = 175$ kV for positive and negative subsystem, respectively.

Within a split-busbar scenario, a three-phase-to-ground fault (f-3ph) in the vicinity of PCC C1p is investigated in order to perform FRT sequences. According to related standards [14], HVdc systems have to provide additional reactive power during ac contingencies in order to counteract the occurring ac voltage depression. Reactive current injection is realized in positive sequence (superscript $+1$) for f-3ph according to the control dynamics stated within [10] for bipolar HVdc systems. In order to adhere to the current limits $i_{\mathrm{PCC}}^{+1,\mathrm{C}xs,\mathrm{max}}$ of the ac current components, the transmission of active power is reduced during ac contingencies by limiting the ac current direct component $i_{\mathrm{PCC,d}}^{+1,\mathrm{C1p}}$ related to the increase of reactive ac current injection $i_{\mathrm{PCC,q}}^{+1,\mathrm{FRT}}$. In rigid bipolar configuration the reduction of active power transfer in one bipolar subsystem inevitably has to coincide with an active power reduction in the other subsystem, as converters of positive and negative subsystem are series-connected to the same dc current circuit. This is realized by a terminal-wide coordinated dynamic current limitation scheme according to (9), which is highlighted in grey boxes within Fig. 3.

$$|i_{\mathrm{PCC}}^{+1,\mathrm{C}xs,\mathrm{max}}| \geq \sqrt{\left(i_{\mathrm{PCC,d}}^{+1,\mathrm{C}xs}\right)^2 + \left(i_{\mathrm{PCC,q}}^{+1,\mathrm{C}xs} + i_{\mathrm{PCC,q}}^{+1,\mathrm{T}x,\mathrm{FRT}}\right)^2} \quad (9)$$

Here, $i_{\mathrm{PCC,q}}^{+1,\mathrm{T}x,\mathrm{FRT}}$ is a terminal-wide determined variable. It represents the maximum absolute value from both reactive current components to realize FRT measures in positive and negative converter. Therefore, an ac contingency in one subsystem leads to an active power reduction in both subsystems. Power reduction on the dc side is achieved by means of simultaneous dynamic limitation of both dc current and ac current direct component. In order to comply with the instantaneous total energy balancing requirements in each converter, injection of balancing ac current components $i_{\mathrm{conv,d}}^{\mathrm{C1}s,\mathrm{bal,ac}}$ remain enabled during contingencies.

Fig. 5 shows the response of a rigid bipolar HVdc link according to operating points stated in Table III to a f-3ph in the vicinity of PCC C1p. Ac current controls according to [10] are realized in rotating reference frame (dq-frame). Therefore, ac quantities are shown in dq-frame as well. The fault occurs at t=1.5 s, considering a fault impedance of 1 mΩ, and is cleared at t=1.75 s. Prior to the failure occurrence, the HVdc system is in steady-state. Due to the implemented transmission loss estimation control block according to Fig. 3 (blue colored box), the dc voltage levels are adapted to $u_{\mathrm{dc}}^{\mathrm{C}x\mathrm{p,ref}} = 518.3$ kV and $u_{\mathrm{dc}}^{\mathrm{C}x\mathrm{n,ref}} = 181.7$ kV for positive and negative subsystem, respectively (see Fig. 5(a)). This adaption enables the transmission of requested active power levels in each bipolar subsystem.

After fault occurrence the ac voltage $u_{\mathrm{PCC,d}}^{+1,\mathrm{C1p}}$ at PCC C1p drops (see Fig. 5(b)), which entails the injection of a dynamic reactive ac current component $i_{\mathrm{PCC,q}}^{+1,\mathrm{C1p,FRT}}$ in positive sequence at PCC C1p (see Fig. 5(e)). Reactive ac current injection at C1p is limited by the overall ac current limit described by (9). Reasoned by a terminal-wide current limitation scheme, the active power transfer is reduced in both subsystems (see Fig. 5(d)-(f)). Nevertheless, unintentional acdc interactions do not occur. As ac quantities of positive and negative converter operate independently, PCC C1n is not affected by this event (see Fig. 5(c)) except for active power reduction. Moreover, injection of reactive current $i_{\mathrm{PCC,q}}^{+1,\mathrm{C1n}}$ at PCC C1n remains at its operation point according to Table III (see Fig. 5(f)). During contingencies the transmission loss estimation block is

deactivated and dc voltage levels are set according to their no load set points (see Fig. 5(a)). The injection of total energy balancing components $i_{\mathrm{conv,d}}^{\mathrm{C1}s,\mathrm{bal,ac}}$ is prioritized during contingencies, which explains the corresponding current behaviour of $i_{\mathrm{PCC,d}}^{\mathrm{C1}s}$ immediately after fault occurrence and clearing in Fig. 5(e)-(f). Therefore, ac as well as dc quantities return to their initial state prior to fault occurrence in the desired manner within approximately 200 ms after fault clearing.

IV. Conclusion

HVdc links in rigid bipolar configuration present a cost-efficient solution to realize bulk power transmission at high system lengths, but uncover new challenges regarding control design. These are traced back to the fact that dc side degrees of freedom are reduced in contrast to bipolar configuration with DMR. Nevertheless, it was elaborated within this contribution that flexible operating conditions are feasible in rigid bipolar configuration, when communication between both terminals is assumed, despite physical restrictions related to the configuration itself. An advanced control and balancing scheme was introduced in order to realize the transmission of different active power levels in each bipolar subsystem in an ac split-busbar scenario. This includes dc voltage as well as dc current control, a power and energy balancing scheme and an adaptive dc voltage reference value determination in order to compensate transmission losses adequately.

The introduced control and balancing scheme was validated by means of EMT simulations. Here, it was proven that FRT requirements according to [14] can be fulfilled despite reduced system degrees of freedom in rigid bipolar configuration. However, an ac contingency inevitably results in an active power reduction in both bipolar subsystems.

Moreover, the applicability of the introduced methodology for subsystem-independent power transfer was discussed for the utilization of different submodule types. MMCs equipped with full-bridge-type submodules enable the realization of this methodology in a flexible manner. HB-MMCs are applicable to a limited extent resulting in a design trade-off between maximum subsystem power difference and current stresses in power electronic devices.

References

[1] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga and R. Teodorescu, *Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems*, Chichester, UK: John Wiley & Sons Ltd, Aug. 2016.

[2] A. Nami, J. Liang, F. Dijkhuizen and G.D. Demetrieades, *Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities*, IEEE Trans. Power Electron., Vol. 30, No. 1, pp. 18-36, Jan. 2015.

[3] M. Saltzer et al., *Surge and extended Overvoltage Testing of HVdc Cable Systems*, presented at the Int. Conf. Insulated Power Cables, Dunkerque, France, Nov. 2017.

[4] M. Callavik, P. Lundberg, O. Hansson, *NORDLINK Pioneering VSC-HVDC Interconnector between Norway and Germany*, white paper from ABB, 2015.

[5] Ø. Sagosen, A. Craig, R. Poole, P. Paradine, *Need, Design and Business Case for Building the North Sea Link*, presented at the CIGRE General Meeting, Paris, France, Aug. 2018.

[6] ENERGINET, *Technical Issues related to new Transmission Lines in Denmark*, Report, Fredericia, Denmark, Sep. 2018.

[7] C. Hirsching et al., *On Control and Balancing of MMC-HVdc Links in Rigid Bipolar Configuration*, presented at the 15th IET International Conference on AC and DC Power Transmission (ACDC), Coventry, United Kingdom, Feb. 05-07 2019.

[8] M. Goertz et al., *Analysis of Overvoltage Levels in the Rigid Bipolar MMC-HVDC Configuration*, presented at the 15th IET International Conference on AC and DC Power Transmission (ACDC), Coventry, United Kingdom, Feb. 05-07 2019.

[9] CIGRÉ WG B4.57, *Guide for the Development of Models for HVDC Converters in a HVDC Grid*, CIGRE Tech. Rep. 604, 2014.

[10] S. Wenig, M. Goertz, C. Hirsching, M. Suriyah and T. Leibfried, *On Full-Bridge Bipolar MMC-HVdc Control and Protection for Transient Fault and Interaction Studies*, IEEE Trans. Power Del., Vol. 33, No. 6, pp. 2864-2873, Dec. 2018.

[11] S. Wenig, *Potential of Bipolar Full-Bridge MMC-HVdc Transmission for Link and Overlay Grid Applications*, Ph.D. dissertation, Dept. Electr. Eng., Karlsruhe Inst. of Techn. (KIT), Karlsruhe, 2019

[12] C. Oates, *Modular Multilevel Converter Design for VSC HVDC Applications*, IEEE Trans. Emerg. Sel. Topics Power Electron., Vol. 03, No. 2, pp. 505-515, Jun. 2015.

[13] CIGRÉ WG B4.46, *Voltage Source Converter (VSC) HVDC for Power Transmission - Economic Aspects and Comparison with other AC and DC Technologies*, CIGRE Tech. Rep. 492, Apr. 2012.

[14] *Technical requirements for grid connection of high voltage direct current systems and direct current-connected power park modules*, E-VDE-AR-N 4131 Std., Mar. 2019.